InGaAs Field-Effect Transistors with Submicron Gates for *K*-Band Applications

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***Abstract*—Depletion mode InGaAs microwave power MISFET's with 0.7 μm gate lengths and 0.2 mm gate widths have been fabricated using an epitaxial process. The devices employed a plasma deposited silicon dioxide gate insulator. The RF power performance at 18 GHz, 20 GHz, and 23 GHz is presented. An output power density of 1.04 W/mm with a corresponding power gain and power-added efficiency of 3.7 dB and 40%, respectively, was obtained at 18 GHz. This is the highest output power density obtained for an InGaAs based transistor on InP at *K*-band. Record output power densities for an InGaAs MISFET were also obtained at 20 GHz and 23 GHz. The output power was demonstrated to be stable within 3% over 17 hours of continuous operation at 18 GHz.**

Introduction

INDIUM gallium arsenide (InGaAs) is a promising electronic material for high frequency applications. $In_{0.53}Ga_{0.47}As$ lattice matched to semi-insulating (SI) indium phosphide (InP) has higher low field mobility (12 000 $cm^2/V\,s$), peak electron velocity (3×10^7 cm/s), and intervalley separation (0.55 eV) than InP or gallium arsenide (GaAs) [1]. Metal-insulator-semiconductor field-effect transistors (MISFET's) fabricated on this semiconductor are, thus, expected to provide superior microwave performance compared to InP MISFET's. However, because InGaAs has lower ionization coefficients and a lower breakdown field than InP, high frequency device operation may be attained at the expense of reduced power output.

Recently, InGaAs MISFET's with 1 μm gate lengths have demonstrated an output power greater than 1 W at 9.7 GHz [2]. An output power density of 1.07 W/mm of gate width was obtained with a corresponding power gain and power-added efficiency of 4.3 dB and 38%, respectively, at an input power of 26 dBm. In addition, excellent output power stability was demonstrated. Over 24 hours of continuous operation, output power was stable to within 1.2%.

There have been very few reports of RF power measurements on InGaAs MISFET's at higher frequencies. Ion-implanted InGaAs MISFET's with 1 μm gate lengths have demonstrated output power densities of 0.40 W/mm and 0.27 W/mm with corresponding power-added efficiencies of 25% and 19% at 10 GHz and 12 GHz, respectively [3]. InGaAs power MISFET's with 1 μm gate lengths have also demonstrated microwave performance in the frequency range from 12 GHz to 32.5 GHz [4]. Output power densities of 0.76 W/mm, 0.74 W/mm, and 0.20 W/mm have been obtained at 12 GHz, 20 GHz, and 32 GHz, respectively. The corresponding power-added efficiencies were 40%, 26%, and 7%.

The potential of InGaAs MISFET's in wide-band power amplifier applications has also been demonstrated [5]. An output power density of 0.47 W/mm with a corresponding gain and power-added efficiency of 6.4 $\pm$ 0.3 dB and 30 $\pm$ 3%, respectively, was obtained over the 7–11 GHz band. In addition, an output power density of 0.39 W/mm with 29 $\pm$ 4% power-added efficiency was obtained over the 6–12 GHz octave band.

This paper reports on the fabrication of 0.7 μm gate length depletion mode InGaAs MISFET's using an epitaxial process. The dc characteristics and RF power performance at 18 GHz, 20 GHz, and 23 GHz are presented. This is the first report of RF power measurements on InGaAs MISFET's with submicrometer gate lengths.

Experimental

The InGaAs MISFET's were fabricated on layers grown lattice matched on semi-insulating (SI) InP substrates using metal organic chemical vapor deposition (MOCVD). An InP buffer layer was grown unintentionally doped to a thickness of 0.2 μm. The thickness of the InGaAs active layer ($n = 2\text{–}3 \times 10^{17}\ cm^{-3}$) was 0.3 μm. The SI-InP (Fe doped) substrates used for the layer growth were liquid encapsulated Czochralski (LEC) grown wafers with a two inch diameter. The surface orientation was (100) misoriented 2° toward the nearest (110) direction.

The layers were grown in a horizontal, low pressure reactor (Aixtron model AIX 200). The precursors for the InP layer growth were trimethylindium (TMIn) and phosphine (PH_3). The precursors for the InGaAs layer growth were TMIn, trimethylgallium (TMGa), and arsine (AsH_3). The dopant source for the InGaAs active layer was diluted silane (2% SiH_4/H_2). Palladium diffused hydrogen was used as a carrier gas. The TMIn and TMGa precursors were transported from stainless steel cylinders with thermostatically controlled temperatures of 17°C and −10°C,

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respectively. The cylinders were electronically pressured controlled for extremely stable evaporation rates.

All gas flows were accurately controlled by electronic mass flow controllers and pneumatically operated valves. For extremely sharp interface formation all precursors were switched by a zero dead volume high speed vent/run switching manifold.

The layers were grown at a reactor pressure of 2000 Pa. The growth temperature was 600°C. The total gas flow rate was adjusted to obtain a gas velocity of 2.2 m/s. For the InP layer growth, the TMIn and PH_3 partial pressures were 0.256 Pa and 148 Pa, respectively. For the InGaAs layer growth, the TMIn, TMGa, AsH_3, and SiH_4 partial pressures were 0.256 Pa, 0.147 Pa, 59 Pa, and 0.055 Pa, respectively.

The growth rates for the InGaAs and InP layers were 2.9 μm/hr and 1.3 μm/hr, respectively. The lattice parameter was matched to within $< \pm 5 \times 10^{-4}$. The InGaAs mobility at 300 K was 5500 cm^2/V s.

A cross section of the InGaAs MISFET fabrication process is shown in Fig. 1. The samples were initially cleaned by first degreasing in acetone and methanol followed by a DI water rinse. The samples were then dipped for 15 s in a 10:1 H_2O:HF solution followed by a DI water rinse and then blown dry in nitrogen. After the initial clean, a mesa etch was performed using a 1:1:38 $H_2SO_4:H_2O_2:H_2O$ solution in order to define the device active area (Fig. 1(a)). Source/drain contacts consisted of Au/Ge 12 wt.% eutectic and Au evaporated to thicknesses of 160 nm and 140 nm, respectively. The contacts were defined using a liftoff technique (Fig. 1(b)). Ohmic contacts were obtained by alloying for 5 min at 400°C in forming gas (10% H_2/N_2). Channel recess etching was then performed using a 1:1:100 $H_2SO_4:H_2O_2:H_2O$ solution (Fig. 1(c)).

After stripping the photoresist, the wafer was again cleaned and a silicon dioxide gate insulator was plasma deposited to a thickness of about 50 nm [6]. The films were deposited using a Technics Planar Etch IIA plasma system modified for 13.56 MHz operation [7]. The silicon dioxide films were deposited at a pressure of 350 mTorr using a 50 W plasma. The substrate temperature was 250°C. The SiH_4 and N_2O flow rates were 19 sccm and 55 sccm, respectively. The gate insulator post deposition treatment consisted of a 300°C anneal for 30 min in a pure hydrogen ambient. The mesa area was then planarized by evaporating silicon dioxide to a thickness of 350 nm and using a liftoff process (Fig. 1(d)). The purpose of the *e*-beam oxide planarization step was to facilitate submicrometer gate length definition in the subsequent photolithographic step.

The gate metal consisted of Ti and Au evaporated to a thickness of 20 nm and 440 nm, respectively, and defined using a liftoff process. Finally, source/drain oxide windows were opened and a Au overlayer was deposited to a thickness of 450 nm using a liftoff process (Fig. 1(e)). The Au overlayer assisted the current handling of the devices and facilitated wire bonding to the drain regions.

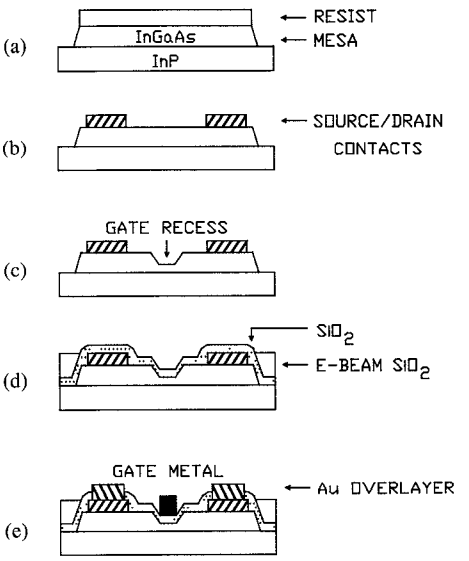

Fig. 1. Cross sections of InGaAs MISFET fabrication process.

The InGaAs MISFET's were prepared for RF packaging by first thinning the sample backside using a (10:1:1) $HCl:HNO_3:H_2O$ solution. The substrates were thinned to about 100 μm to improve the thermal resistance and then scribed into individual MISFET's. Backside metallization was then performed by evaporating Ti and Au to a thickness of 20 nm and 450 nm, respectively, in order to aid heat dissipation of the MISFET's.

For the RF power measurements, the devices were mounted on a test fixture using silver epoxy and subsequently wire bonded. The test fixture consisted of input and output microstrip circuits applied to a gold-plated brass block using a sweat soldering technique. The microstrip circuits contained a RF choke for applying dc bias while chip capacitors were used as dc blocks across microstrip gaps. Electrical connections between the test fixture microstrip and measurement system were made using 2.4 mm coax to microstrip launchers. Impedance matching was done empirically using external metal stubs close to the transistor. The details of the test fixture have been described previously [8]. The results reported below have been corrected for fixture losses.

Results

The completed InGaAs MISFET's had 2 parallel gate fingers with individual gate widths of 100 μm. The individual gate finger width was limited to the above values in order to avoid possible gain degradation associated with larger gate widths [9]. The total gate width was 0.2 mm. The separation between the gate fingers was 114 μm. The large spacing between the gate fingers was necessary in order to facilitate wire bonding to the individual drain regions. The source/drain contact spacing was 5 μm and the length of the gate recess was 1 μm. The device gate length was 0.7 μm.

The *I–V* characteristics of an InGaAs MISFET with a silicon dioxide gate insulator are shown in Fig. 2. The

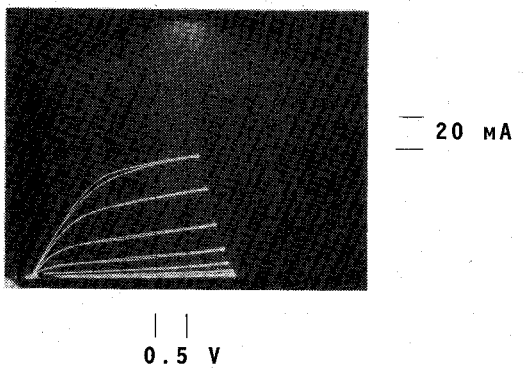

Fig. 2. *I–V* characteristics of InGaAs MISFET. Horizontal: 0.5 V/div. Vertical: 20 mA/div. Gate (V_{gs}): −2 V/step.

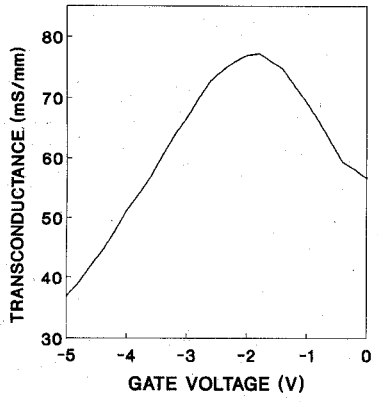

Fig. 3. Transconductance versus gate voltage (V_{ds} = 2.5 V).

gate voltage range is from 0 V to −14 V in −2 V steps. At a drain-source bias of 2.5 V, the drain saturation current was 75 mA. The devices had typical source-drain breakdown voltages of 6–8 V. The gate-drain and gate-source breakdown voltages were greater than 20 V.

Fig. 3 shows the device transconductance per unit gate width as a function of gate-source voltage. The results were obtained using a HP4145B Semiconductor Parametric Analyzer. The drain-source bias was 2.5 V. The peak transconductance typically occurred at a gate-source bias of about −2 V. The maximum device transconductance was typically about 70–80 mS/mm.

The results of a drain current drift measurement of an InGaAs MISFET with a silicon dioxide gate insulator is shown in Fig. 4. Prior to the start of the measurement, the drain-source and gate-source biases were 2.0 V and 0 V, respectively, and the drain current was 88.3 mA. At the start of the measurement, the gate-source bias was switched to −2.0 V. The initial drain current was 60.0 mA. The drain current stabilized after about 1000 s. The drain current variation over a period of 10 000 s was 5.8%. The amount of drain current drift is less than other reports on InGaAs MISFET's with silicon dioxide gate insulators [10], [11]. Recently, a drain current drift of 4% over a period of 10 000 s has been reported for 1 μm gate length InGaAs MISFET's with a silicon/silicon dioxide gate insulator [2]. Reduced drain current drift is, thus,

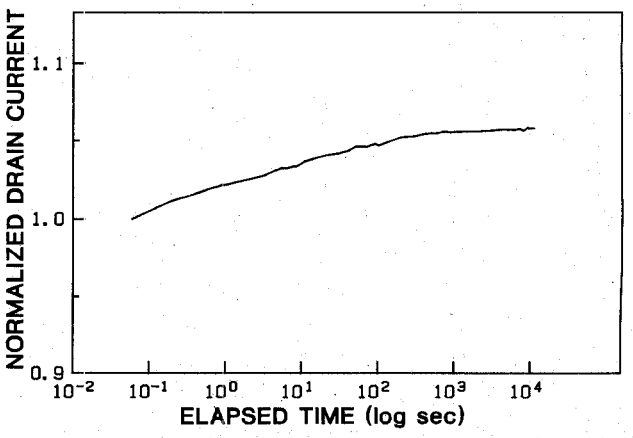

Fig. 4. Drain current drift measurement of InGaAs MISFET with silicon dioxide gate insulator.

being investigated for submicrometer gate length InGaAs MISFET's using plasma deposited silicon dioxide with a thin silicon interfacial layer as a gate insulator.

Fig. 5 shows the output power and power-added efficiency as a function of input power from 9 dBm to 19.5 dBm for a 0.7 μm gate length InGaAs MISFET with a total gate width of 0.2 mm. The measurements were performed at a frequency of 18 GHz using a gate-source bias of −3.5 V and a drain-source bias of 6.0 V. The device saturation current density was about 570 mA/mm of gate width. The linear gain was about 8.5 dB. An output power density of 1.04 W/mm was obtained at an input power of 19.5 dBm. The corresponding gain and power-added efficiency were 3.7 dB and 40%, respectively. To our knowledge, this is the highest output power density obtained for an InGaAs based transistor on InP at *K*-band. The highest power-added efficiency obtained was 45% with a corresponding power gain and output power density of 5.8 dB and 0.95 W/mm, respectively, at an input power of 17 dBm.

The gain compression curve obtained at 20 GHz using gate-source and drain-source biases of −2.5 V and 5.5 V, respectively, is shown in Fig. 6. The linear gain was about 6.1 dB. An output power density of 0.88 W/mm was obtained with a corresponding power gain and power-added efficiency of 3.0 dB and 32%, respectively, at an input power of 19.5 dBm. The highest power-added efficiency obtained was 35% with a corresponding power gain and output power density of 4.2 dB and 0.83 W/mm, respectively, at an input power of 18 dBm. The output power densities obtained are record performances for an InGaAs MISFET at 20 GHz.

Output power measurements were also performed at a frequency of 23 GHz. The results obtained using gate-source and drain-source biases of −3.5 V and 5.8 V, respectively, are shown in Fig. 7. The linear gain was about 5.1 dB. An output power density of 0.74 W/mm was obtained at an input power of 18.5 dBm. The corresponding gain and power-added efficiency were 3.2 dB and 27%, respectively. The highest power-added efficiency obtained was 28% with a corresponding power gain and out-

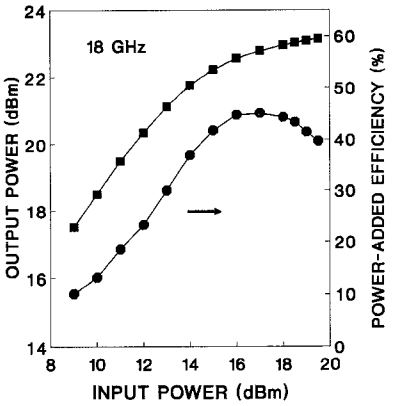

Fig. 5. Output power, power-added efficiency versus input power at 18 GHz (V_{ds} = 6.0 V, V_{gs} = −3.5 V).

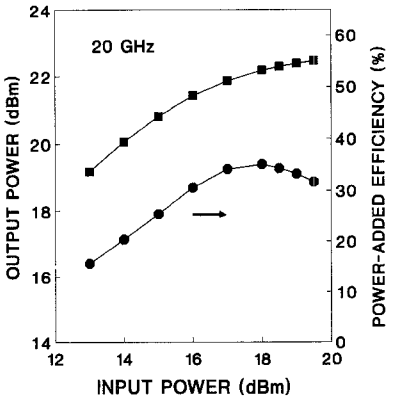

Fig. 6. Output power, power-added efficiency versus input power at 20 GHz (V_{ds} = 5.5 V, V_{gs} = −2.5 V).

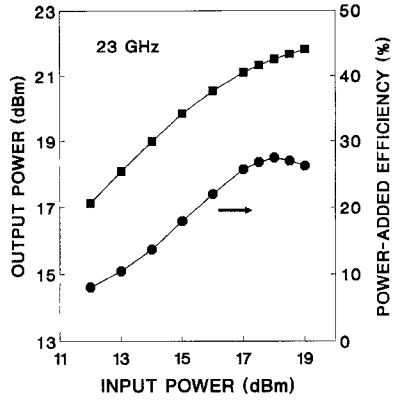

Fig. 7. Output power, power-added efficiency versus input power at 23 GHz (V_{ds} = 5.8 V, V_{gs} = −3.5 V).

put power density of 3.5 dB and 0.71 W/mm, respectively, at an input power of 18 dBm. This is the first report of submicrometer gate length InGaAs MISFET's with high output power performance up to 23 GHz.

Of technological significance is the fact that the drain bias current of these devices can be decreased and maintained for extended periods with negative gate bias at a fixed drain bias. The control of drain bias current through the use of a negative gate bias allowed the device output

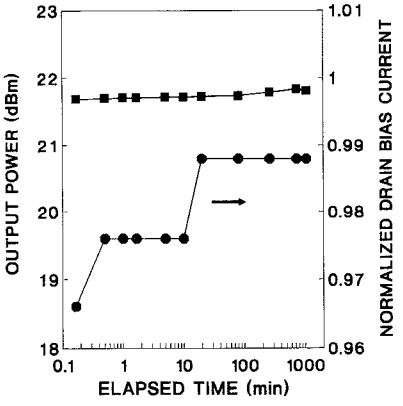

Fig. 8. Time dependence of output power and drain bias current at 18 GHz.

power to be optimized for the record output power densities reported here.

The output power stability of these devices was also investigated. The output power and normalized drain bias current (I_{ds}/I_{dso}) variation of a representative device over a 17 hour period is shown in Fig. 8. The measurement was performed at 18 GHz. Prior to the start of the measurement, the gate-source and drain-source biases were 0 V. At the start of the measurement, an RF input power, gate-source bias, and drain-source bias of 16.2 dBm, −4.0 V, and 5.0 V, respectively, were applied. The initial drain bias current was 50.1 mA. The output power and drain bias current variation were 3% and 3.4%, respectively, over a 17 hour period. The variation may be due to insulator interfacial traps and may be further reduced by using a thin silicon interfacial layer [2], [6], [10].

Summary

Depletion mode InGaAs MISFET's with 0.7 μm gate lengths and 0.2 mm gate widths were fabricated using an epitaxial process. At 18 GHz, microwave power transistors produced an output power density of 1.04 W/mm with a corresponding power gain and power-added efficiency of 3.7 dB and 40%, respectively. The highest power-added efficiency was 45% with a corresponding output power density of 0.95 W/mm and power gain of 5.8 dB. At 20 GHz and 23 GHz, output power densities of 0.88 W/mm and 0.74 W/mm, respectively, were obtained. The highest power-added efficiencies obtained at 20 GHz and 23 GHz were 35% and 28%, respectively. In addition, output power was demonstrated to be stable within 3% over 17 hours of continuous operation. This is the first report of RF power measurements on InGaAs MISFET's with submicrometer gate lengths. An output power density greater than 1 W/mm has been demonstrated for the first time for an InGaAs based transistor on InP at *K*-band. In addition, the output power densities obtained are the highest reported for an InGaAs MISFET at *K*-band. Further improvements are expected by optimizing the device structure. Presently, enhanced device performance is being investigated by reducing the device

source/drain spacing. In addition, improved drain current drift and output power stability are being investigated using a silicon dioxide gate insulator with a thin silicon interfacial layer [2], [10].

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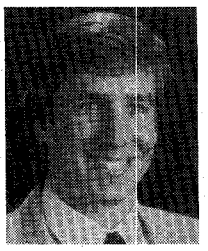

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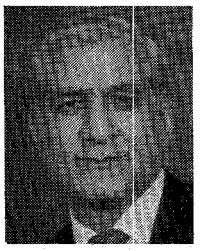

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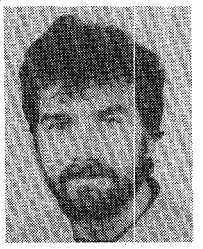

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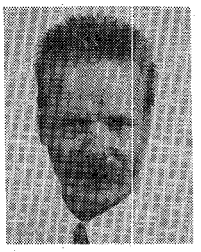
He worked as a student staff member of the III-V compound semiconductors VPE-group at the Technical University of Aachen from 1981 through 1984. He joined AIXTRON Semiconductor Technologies in Aachen in 1984. He has been the head of process development at AIXTRON in 1986.



Holger Jurgensen attended the Technical University in Aachen, Germany, where his research included the epitaxial growth of InP films, and growth investigations of GaInAs/InP-multi-layer structures.

He worked as a staff member at the Institute of Semiconductor Electronics in the Solid State Electronics department while he was a student at the Technical University. His research included vapor phase deposition and characterization of III-V compound semiconductor films for microwave and optoelectronic applications. He joined AIXTRON Semiconductor in Aachen, Germany as President and Technical Director in 1983.

He was the recipient of the Award for Technology Transfer from the German Federal Secretary of Culture and Science in 1986, and the Award for Innovations from the Minister for Research and Technology in Germany in 1988.